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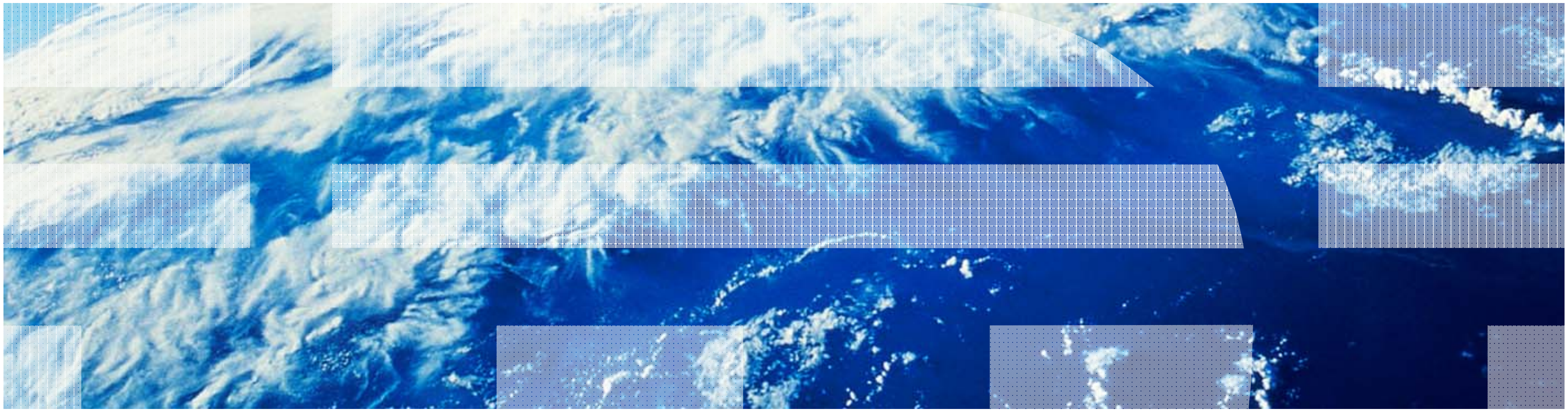
# Technology Roadmap Comparisons for TAPE, HDD, and NAND Flash: Implications for Data Storage Applications



# Outline

- **Business as Usual Areal Density Increase → 40% per Year**
- **Premise: The annual rate of areal density increases for TAPE will likely exceed the annual rate of areal density increases for NAND and HDD**
  - TAPE bit cell is large and paths for scaling to higher bit densities exist
  - NAND bit cells and HDD Patterned Media bit cells are approaching nanoscale issues in minimum feature lithography requirements
  - NAND bit endurance or bit retention and HDD bit stability are approaching kT fluctuation issues driven by the small volume of the bit cells at high areal densities ( < 1900 $nm^2$ bit cell area)
- **Comment: TAPE, NAND, and HDD will continue to offer complementary storage solutions**
- **Implications for TAPE: TAPE volumetric density will increase, allowing for new tape opportunities in a more cost sensitive storage environment**
- **A Possible Annual Areal Density Growth Scenarios**
  - ~ 20% for HDD
  - ~ 20% for NAND Flash
  - > 40% for TAPE

# Outline NEW

- **Areal density landscape for TAPE, HDD, NAND**
- **Bit cells**
- **Lithography and / or bit cell definition**
- **TAPE , NAND, HDD landscapes**
- **Areal density increase scenarios for the next 4 year period**
- **Conclusions**

# Storage Component Landscape

- **Three Components**
  - HDD ~ 500 GB capacity 630 million units/yr (large commodity base)
  - NAND Chip ~ 4 GB capacity 4 billion units/yr (large commodity base)
  - LTO Tape Cartridge ~ 800 GB capacity 24 million units/yr (**no commodity base**)

- **The Industries**

| | 2010 | 2011 |
|---|---|---|
| HDD Revenue | $33.5 B | $33.5 B |
| HDD PB Shipped | 330000 PB | 330000 PB |
| HDD $/GB Shipped | $0.10/GB | $0.10/GB |
| NAND Revenue | $18.5 B | $21.5 B |
| NAND PB Shipped | 10,400 PB | 18,600 PB |
| NAND $/GB | $1.77/GB | $1.16/GB |
| TAPE LTO Cartridge Revenue | $0.7 B | $0.7B |
| TAPE LTO Cartridge PB Shipped | 15,300 PB | 17,800 PB |
| TAPE LTO Cartridge $/GB | $0.046/GB | $0.038/GB |

***Thailand Floods***
***Industry Consolidation***

***Transition from 30 nm***
***to 20 nm Lithography***

***Introduction of LTO5***
***Tape Generation***

## Areal Density Overview (a moving target -- concentrate on YE 2011 values)

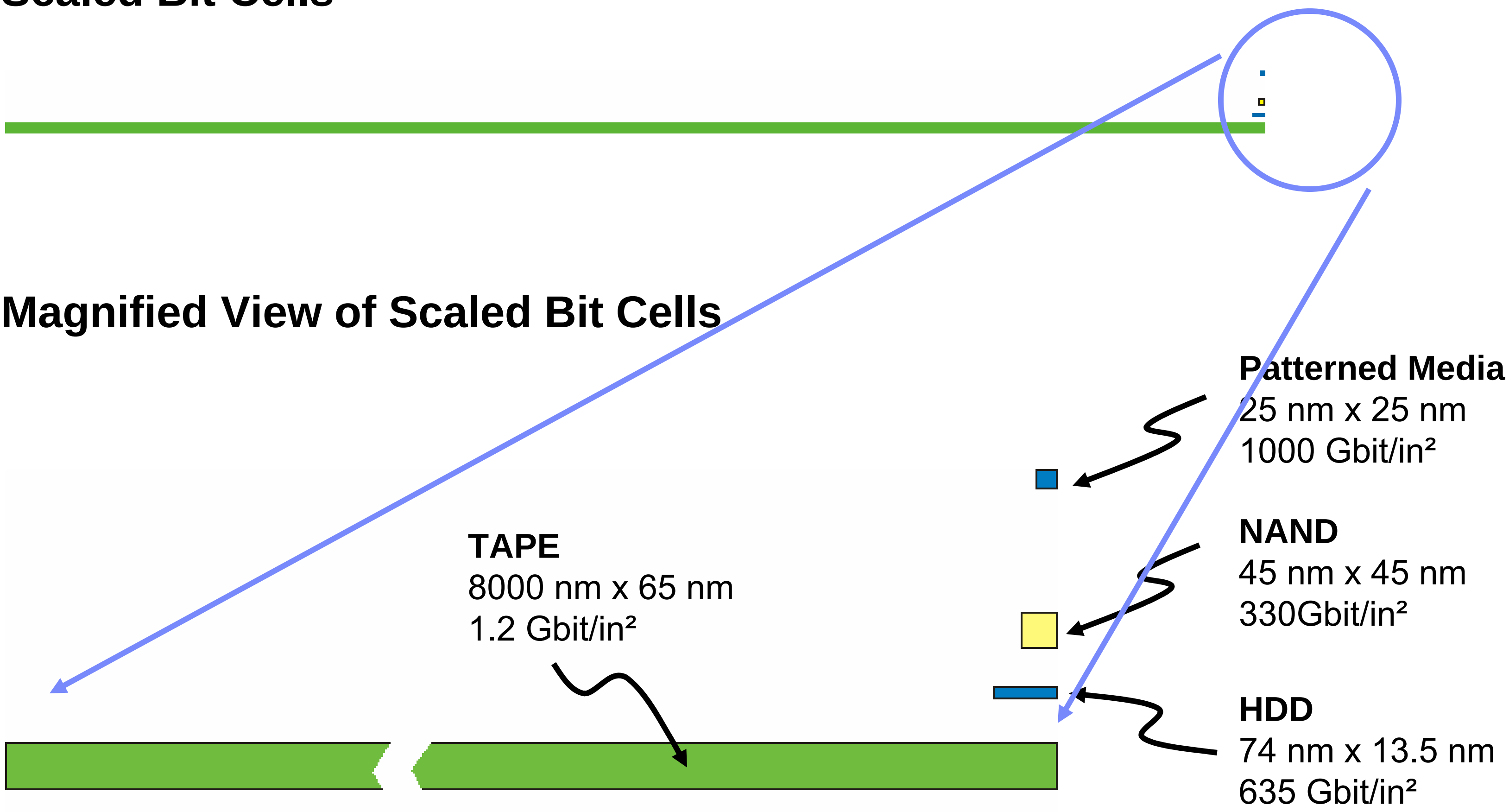
- **HDD (20% - 30%) / Year)**
  - YE 2009 530 Gbit/in²
  - YE 2010 635 Gbit/in²
  - Mid 2011 750 Gbit/in²
- **TAPE (40% / Year)**
  - Mid 2008 1.0 Gbit/in²
  - Mid 2010 1.2 Gbit/in²
  - Mid 2011 3.2 Gbit/in²
- **NAND (40% / Year)**
  - Mid 2008 200 Gbit/in²
  - Mid 2010 330 Gbit/in²
  - Mid 2011 550 Gbit/in²

- **HDD (3.5" Platter)**
  - 750 GB → 1.0 TB
- **TAPE (LTO like Cartridge)**
  - 1.5 TB → 4.0 TB
- **NAND (Chip )**
  - 8 GB → 8 GB with 40% less area)

# Storage Bit Cells and Extendability

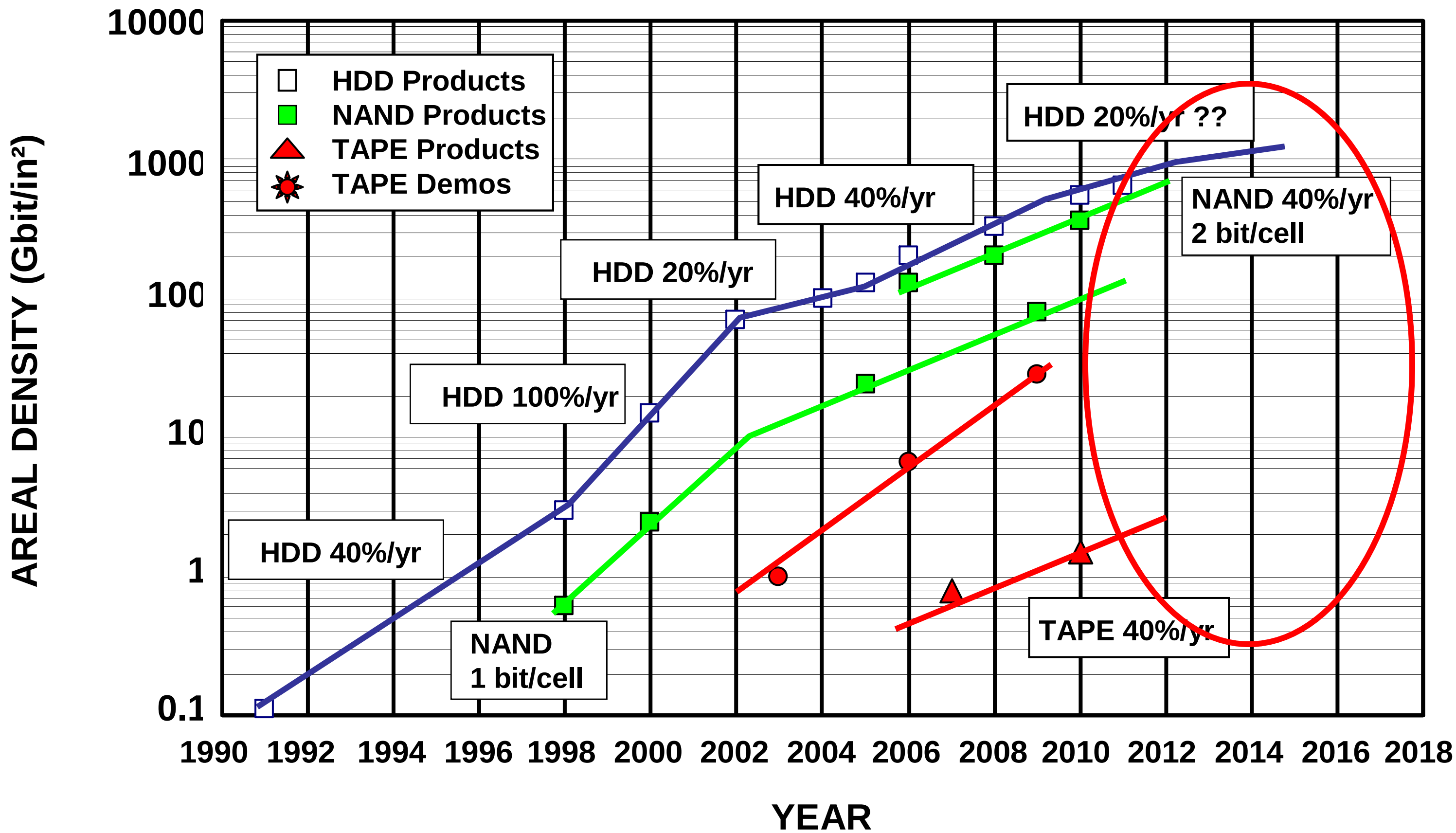
- **Scaled Bit Cells**

- **Magnified View of Scaled Bit Cells**



# Storage Device Density Landscape – A History

- **HDD**
  - 1998 – 2002 density increases at 100% per year (GMR)
- **TAPE**
  - Sustained 40% density increases with demos showing potential for greater increases
- **NAND**
  - 2005 -- transition to 2 bit/cell technology (endurance sacrifice)

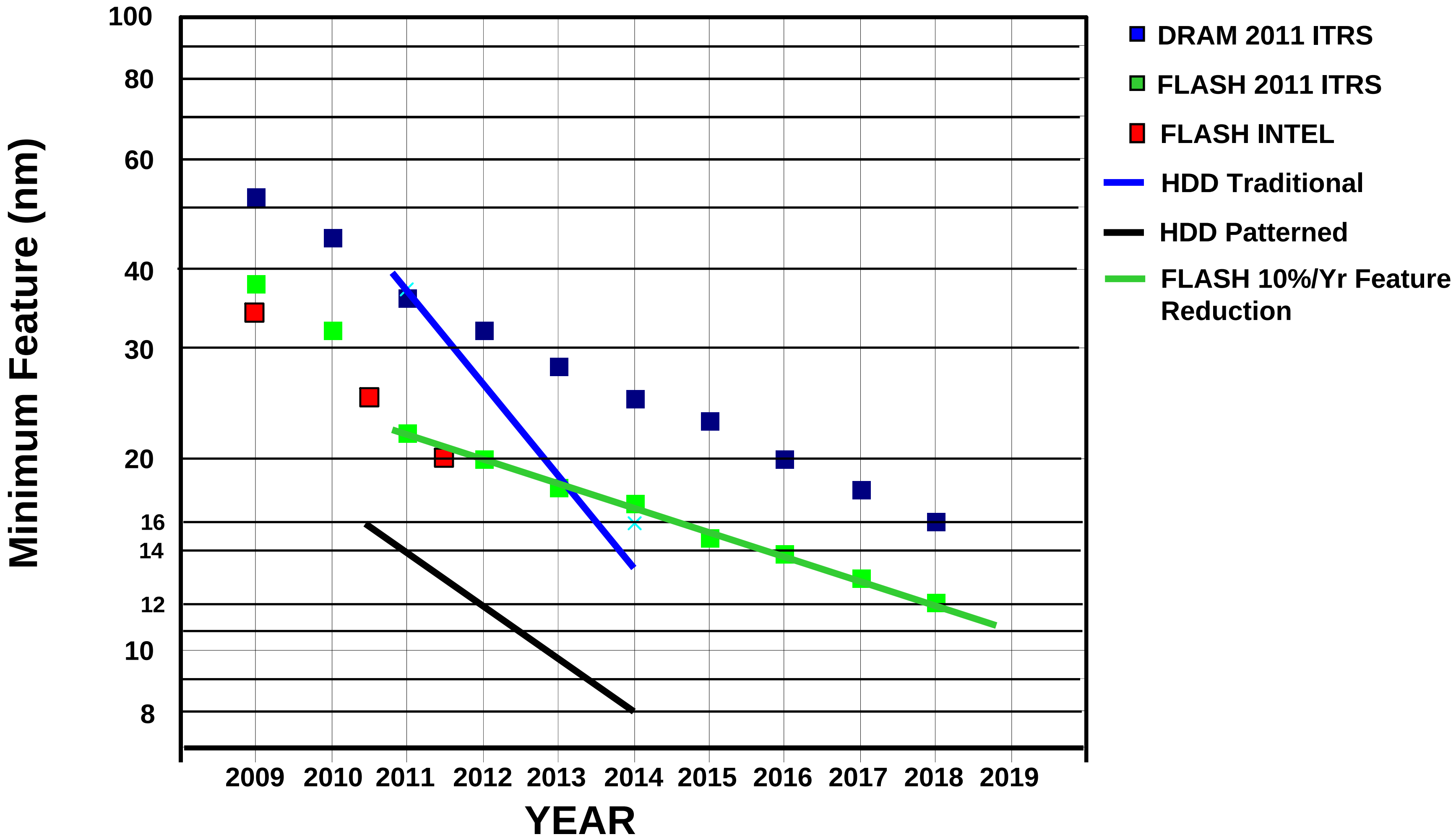


# Bit Cell Implications for 40% Annual Areal Density Increases

| TECHNOLOGY METRIC | 2010 | 2014 (40% / Yr) |
|---|---|---|
| TAPE | | |
| -- Areal Density | 1.2 Gbit / in² | 4.8 Gbit / in² |
| -- Bit Length | 8000 nm | 2000 nm |
| -- Bit Width | 65 nm | 65 nm |
| -- Minimum Feature | 4000 nm | 1000 nm |
| HDD | | |
| -- Areal Density | 635 Gbit / in² | 2500 Gbit / in² |
| -- Bit Length | 74 nm | 19 nm |
| -- Bit Width | 13.5 nm | 13.5 nm |
| -- Minimum Feature | 37 nm | 10 nm |
| NAND Flash | | |
| -- Areal Density | 330 Gbit / in² | 1300 Gbit / in² |
| -- Bit Length | 45 nm | 20 nm |
| -- Bit Width | 45 nm | 20 nm |
| -- Minimum Feature | 25 nm | 12 nm |

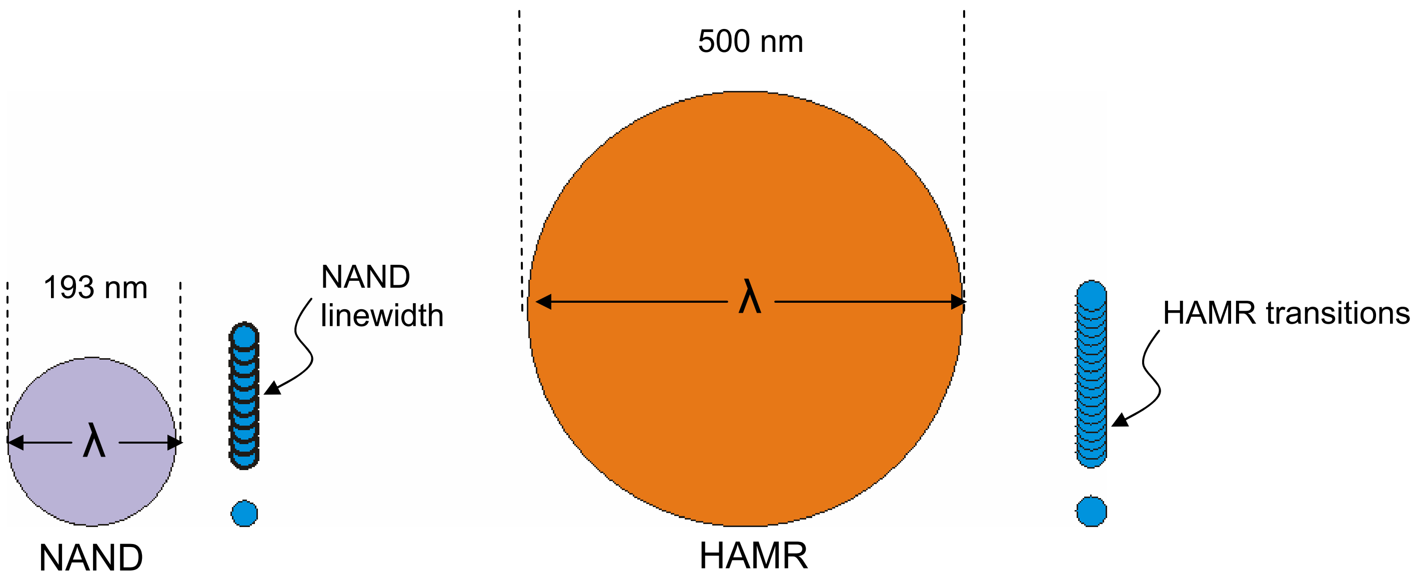
## Lithography Roadmaps

- **Minimum feature typically reduced by 12% per year**
- **Intel/Micron has consistently exceeded ITRS goals**



# NAND and HAMR Optics -- Today

- **NAND uses 193 nm wavelength light to resolve 20 nm features**
  - Phase shift masking
  - Immersion lithography
  - Double exposure at 2X line pitch
  - Chemically amplified resists
- **HAMR uses ~ 500 nm wavelength light to resolve 100 nm features today and 35 nm features for 2 Tbit/in² in the 2014 time frame**
  - Waveguide propagation
  - Waveguide termination with aperture feature (minimum feature)
  - Near field thermal effects
  - Media layer heat sinking

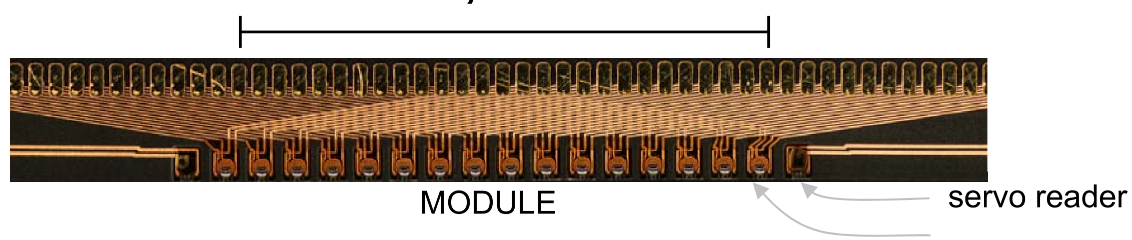


# TAPE Landscape – 1.5 TB LTO-5 Tape Cartridge

- **Tape data storage capacity achieved using 840 m tape length, 12.8 mm wide, and 6.4 um thick**
  - Tape surface area in a cartridge (10.5 x $10^6$ $mm^2$) is equivalent to 148 12” Si wafers or 1736 3.5” disk surfaces
  - Some surface area utilized for edge guards, servo tracks, leading and trailing tape end lengths leading to surface storage efficiencies of ~ 65%

- **1.5 TB LTO-5 Cartridge Details**
  - Areal Density (Maximum) → 1.2 Gbit/in² (0.72 Gbit/in² average density)
  - Total Tracks → 1280
  - Trackwidth → 8100 nm or 8.1 um
  - Bit Length → 65 nm (Bit Aspect Ration = 125!!)
  - TPI, BPI → 3.1 KTPI, 385 KBPI
  - Read Width/Minimum Feature → ~ ½ Trackwidth, ~ 4.0 um
  - Memory Cell Area ($F^2$) → ~ $0.03F^2$ !!!

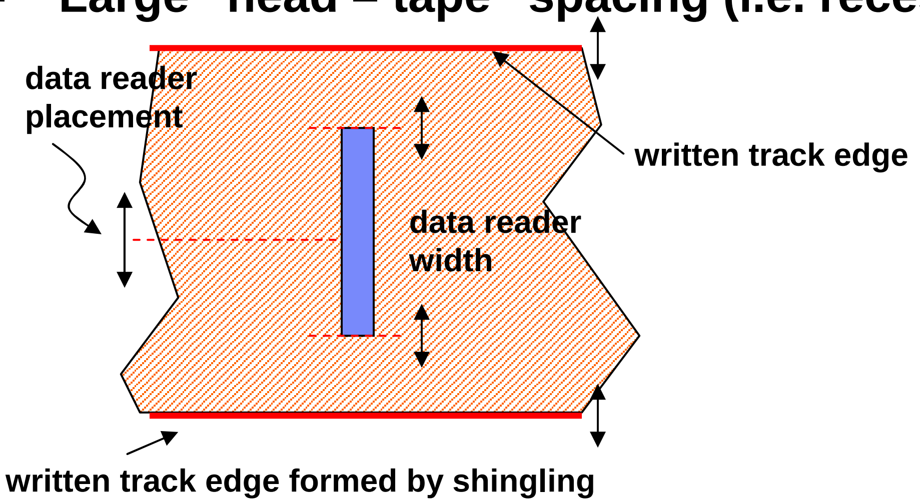
- **The Head – 16 tracks, 2 servo elements**

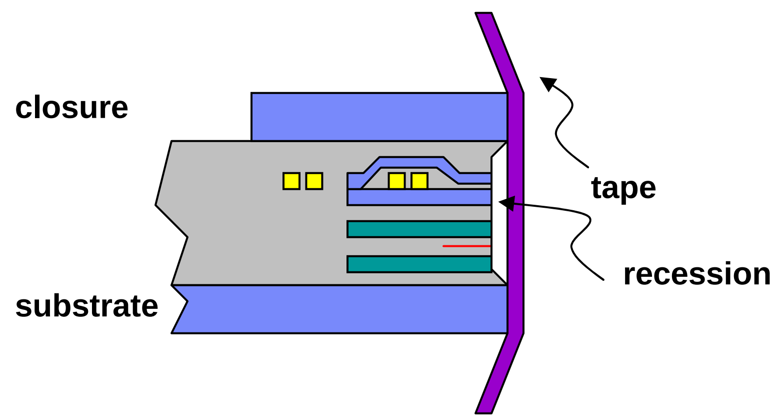


- **Media** -- Recording demonstrations suggest that tape areal densities in excess of 25 Gb/in² can be supported **(20X).** SNR is the issue
- **Head** -- The transition to GMR based sensors provides path for maintaining amplitude as trackwidth decreases and present trackwidths and MR widths in the 4 um range are **200X** larger than present IC minimum features (20 nm); lithography limits are non issues
- **Bit Cell** -- The volume of the bit cell is large so kT fluctuations are minimal and bits are stable. TAPE heads use ***proven*** HDD technology of 12 years ago.

**CAVEATS**

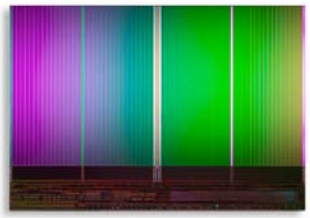
- **Flexible media and track following**
- **Large "head – tape" spacing (i.e. recession changes during head lifetime)**



# Intel Micron 8 GB NAND Chip (2 bit per cell)

**8 GB 20 nm IM Flash**




- Chip Area → 118 mm² (12.5 mm x 9.5 mm)
- Active Memory Area → 71 mm² (63% efficiency)
- Minimum Feature (F) → 20 nm
- Memory Cell Area → 1109 nm²
- Memory Cell Area → 2.8 $F^2$ (not 2 $F^2$ !!!)
- Local Areal Density → 560 Gb/in²

- **NAND Scenario – 10%/year minimum feature decrease, $1500 cost per 12" wafer**

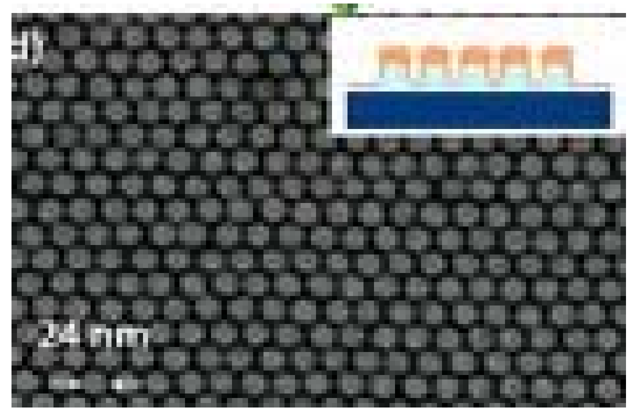
| | 2010 | 2011 | 2013 | 2015 (?) |
|---|---|---|---|---|
| Device Capacity | 8 GB | 8 GB | 16 GB | 32 GB |
| Minimum F | 25 nm | 20 nm | 16 nm | 12.5 nm |
| Areal Density | 330 Gbit/in² | 550 Gbit/in² | 660 Gbit/in² | 1330 Gbit/in² |
| Devices / 300 mm Wafer | 364 | 522 | 364 | 364 |
| TB on 300 mm Wafer | 2.9 TB | 4.2 TB | 5.8 TB | 11.2 TB |
| $ / GB at Wafer Level | $0.52 | $0.36 | $0.26 | $0.13 |

- **What could change? Transition to 3 bit per cell (8 voltage states) design. There is a reason why Intel Micron did not do this at the 25 nm node. 3D options but with larger features.**

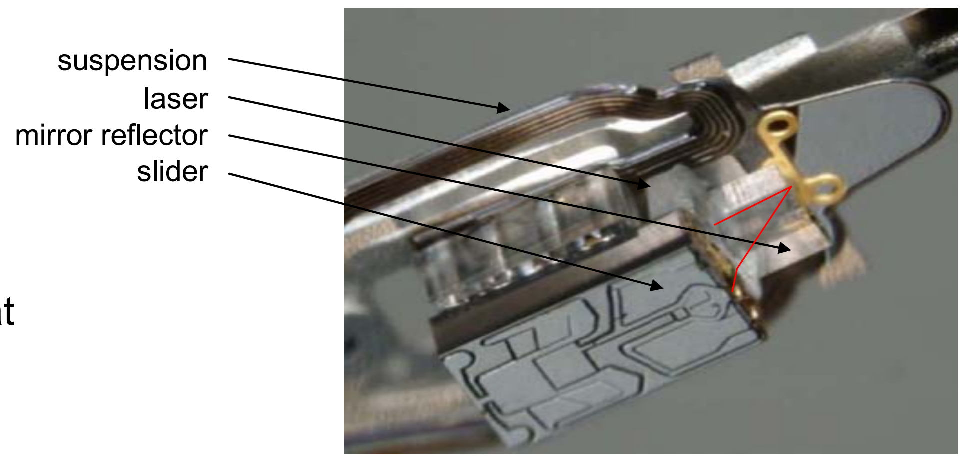
# HDD Landscape – 750 GB Platter (3.5" disc, 2 surfaces)

- **Platter capacity (GB) for a 3.5" disk ~ 1.2 to 1.4) X areal density system**
  - ➔ 635 Gbit/in² areal density supports 750 GB platter
  - ➔ 720 Gbit/in² areal density supports 1000 GB platter
- **750 GB platter details**
  - Areal Density (Maximum) ➔ 635 Gbit/in²
  - Trackwidth ➔ 74 nm
  - Bit Length ➔ 13.5 nm
  - TPI/BPI ➔ 338 KTPI, 1850 KBPI
  - Minimum Feature F ➔ 37 nm (MR sensor width)
  - Memory Cell Area ➔ 4.0 F²
- **Continued 40% annual areal density increases will eventually require minimum features sizes for the MR sensor with smaller dimensions than semiconductor roadmap projections. *Fortunately MR sensors are isolated structures.***
- **The HDD Industry is in transition and anticipate density doubling every 5 years, i.e. 18% per year with the eventual introduction of patterned media and / or heat assisted recording**

# HDD Landscape – Two Strategies




- **Media patterning strategies rely on introduction of imprint technology, a semiconductor roadmap strategy for 2014**
  - E-beam lithography at 1X for master stencils
  - Patterning/Planarization/Stencil development and infrastructure → COST and TIME
  - Major system changes to accommodate bit location and shingle writing
- **Energy assisted strategies must define trackwidths, ~ 2X MRw, using heat, by adding additional components onto the head slider**
  - New media
  - Thermal reliability for media overcoat and heat transducer
  - Laser supply chain
- **Any new technology must be sustainable in the 2.5 Tbit/in² environment**

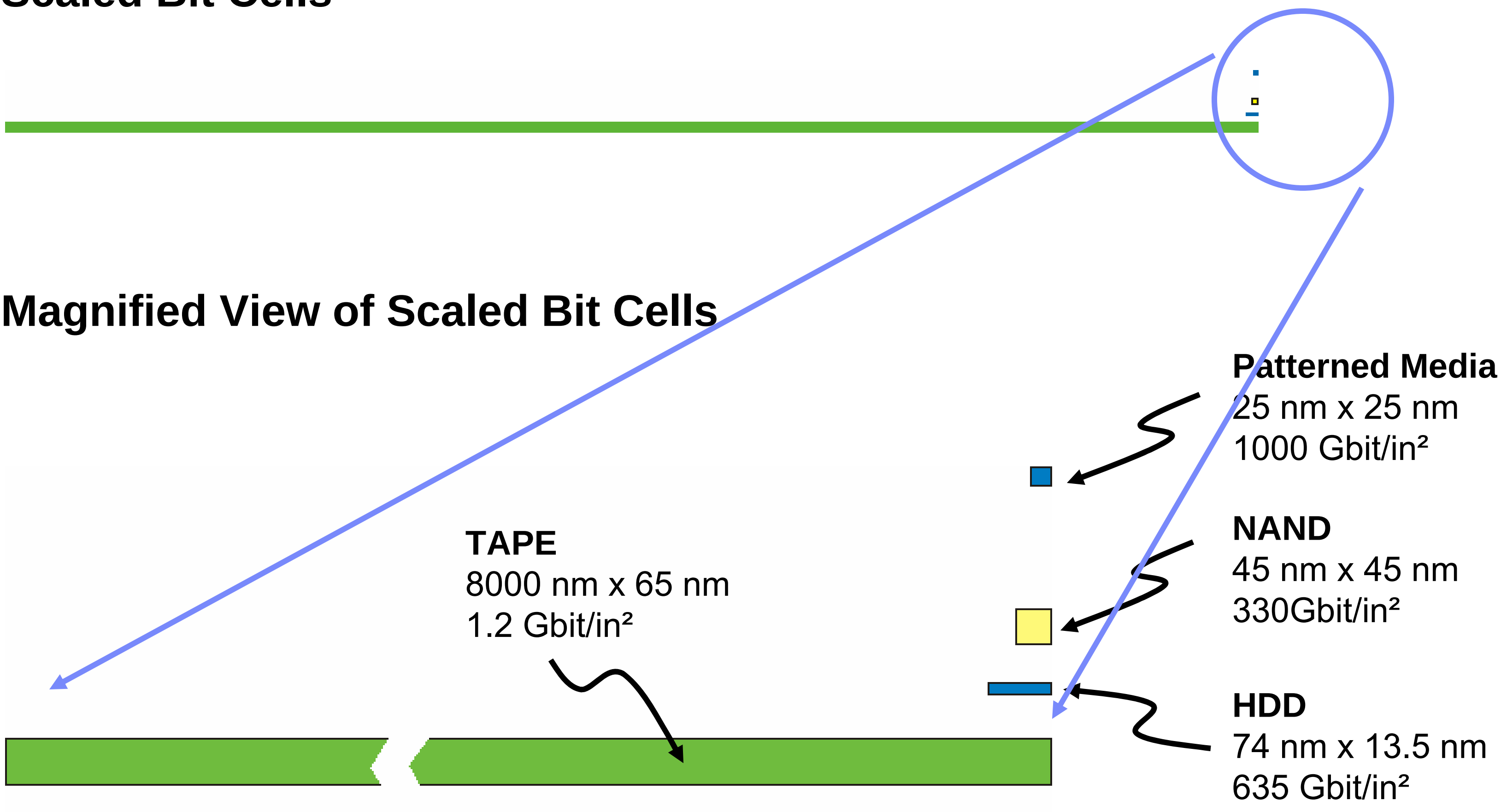



M. Re, "Has HAMR reached a critical mass", The Information Storage Industry Consortium Symposium on Alternative Storage Technologies, April 2009, www.insic.org

# Storage Bit Cells and Extendability

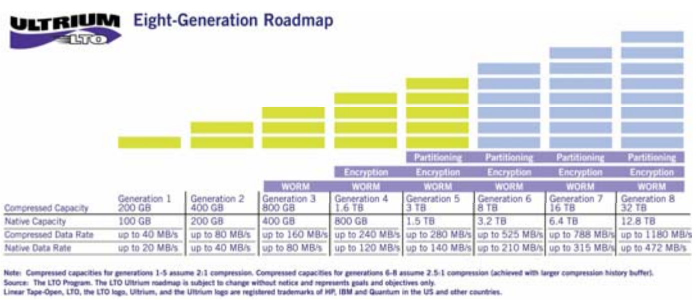
- **Scaled Bit Cells**

- **Magnified View of Scaled Bit Cells**



# Areal Density Scenarios relative to 2014

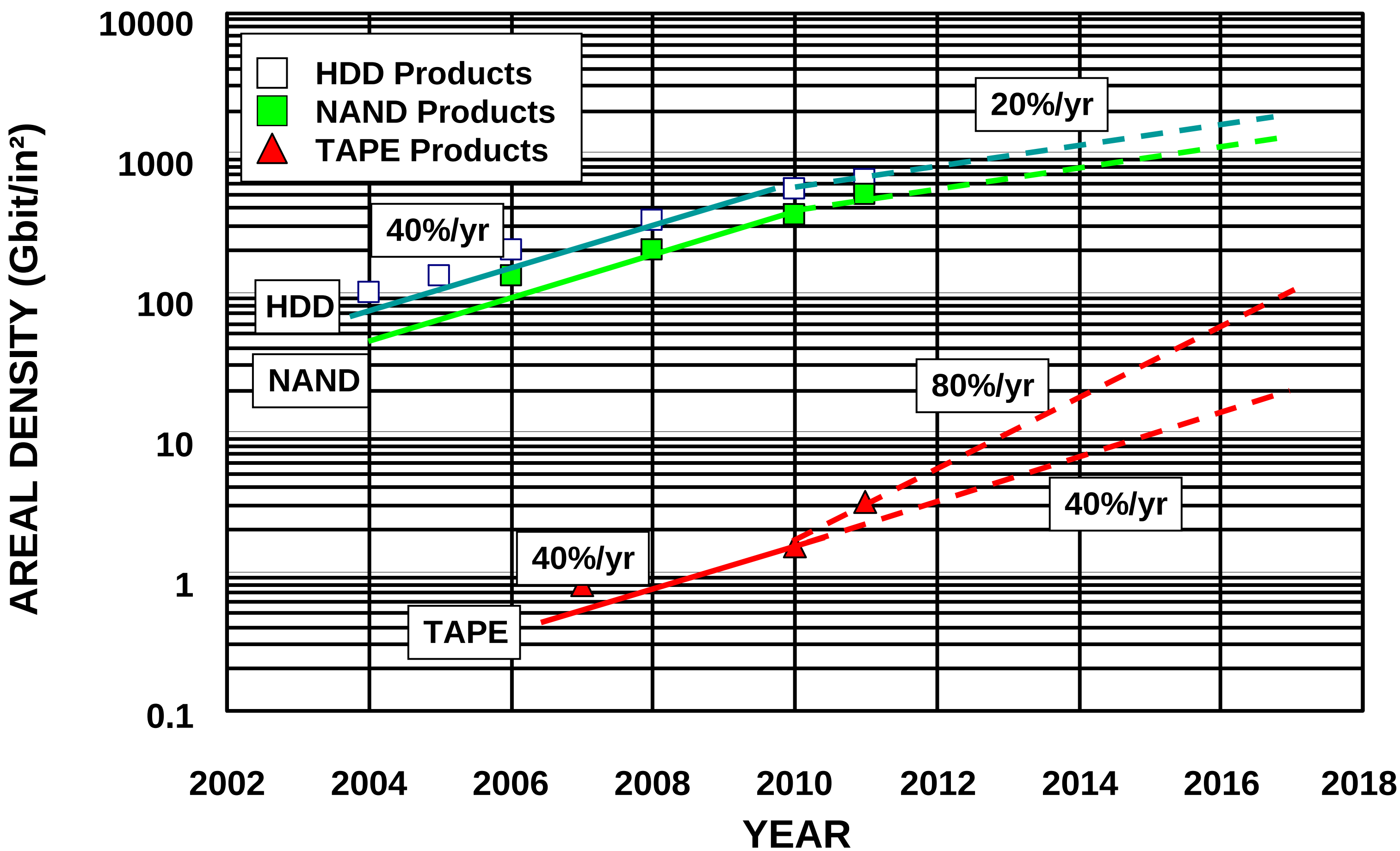
- **HDD**
  - <u>Conservative</u>: 20% density increases achievable
  - <u>Aggressive</u>: 30% density increases are challenging (shingling interim solution)
- **NAND Flash**
  - <u>Conservative:</u> 20% density increases are achievable given the lithography roadmap strategies project reducing feature size 10% annually
  - <u>Aggressive</u>: Sustained 30% density increases are difficult given the conventional understanding of lithography roadmaps and optical processing tooling strategies.
- **TAPE**
  - <u>Conservative</u>: 40% density increases achievable with anticipation of following the LTO Roadmap presently at Generation 5
  - <u>Aggressive</u>: 80% density increases are possible since the needed transducer technology presently exists in the HDD environment but “mechanical” issues related to positioning, wear, and tape stability must be addressed – not NANOSCALE issues




| | Generation 1 | Generation 2 | Generation 3 | Generation 4 | Generation 5 | Generation 6 | Generation 7 | Generation 8 |
|---|---|---|---|---|---|---|---|---|
| Compressed Capacity | 200 GB | 400 GB | 800 GB | 1.6 TB | 3 TB | 8 TB | 16 TB | 32 TB |
| Native Capacity | 100 GB | 200 GB | 400 GB | 800 GB | 1.5 TB | 3.2 TB | 6.4 TB | 12.8 TB |
| Compressed Data Rate | up to 40 MB/s | up to 80 MB/s | up to 160 MB/s | up to 240 MB/s | up to 280 MB/s | up to 525 MB/s | up to 788 MB/s | up to 1180 MB/s |
| Native Data Rate | up to 20 MB/s | up to 40 MB/s | up to 80 MB/s | up to 120 MB/s | up to 140 MB/s | up to 210 MB/s | up to 315 MB/s | up to 472 MB/s |

# Annual Areal Density Growth Rate Scenarios

- **HDD – Transition to New Technology, Sensor Output, Lithography**
- **NAND Flash – Lithography and Endurance**
- **TAPE – No Lithography Issues, Mechanical Realities**



# Summary

- **Density Increases**
  - Tape ➔ > 40% per year building on HDD **existing** technology, no nano-scale issues
  - HDD ➔ 20% per year requiring **revolutionary** technologies
  - NAND ➔ 20% per year with evolutionary lithography
    ➔ > 20 % per year with low endurance multi-bit cells

- **TAPE differences relative to NAND and HDD**
  - Bit cell is 200X larger ➔ thermal kT fluctuations do not impact endurance / bit stability
  - Media thickness is 200X thinner ➔ comparable volumetric densities at component level
  - Lithography requirements not dependent on semiconductor roadmap innovations

- **Numbers**
  - Today's lithographic features are **20 nm**; achieving **16 nm** is difficult for NAND and HDD
  - Areal Densities: HDD ~ **730 Gbit/in²**, NAND ~ **550 Gbit/in²**, TAPE ~ **2 Gbit/in²**
  - NAND cost is **10X** greater than HDD cost. HDD cost is **2.5X** greater than TAPE cost
  - Moore's Law, i.e. capacity doubling per unit area every two years (**40% per year**), will change for NAND and HDD